SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor device, and in particular to a semiconductor device that includes complementary field-effect transistors comprising n-channel field-effect transistors and p-channel field-effect transistors.

Description of the Related Art

In recent years, the processing power demanded of semiconductor devices, such as LSI, has become harsh in accompaniment with the development of information communication equipment, and the working speed of transistors is being increased. In particular, complementary field-effect transistors configured by n-channel field-effect transistors and p-channel field-effect transistors are being widely used because of their low power consumption. Increases in the speed of such transistors have advanced mainly due to the miniaturization of their structures, and have been supported by the progress of lithographic technology for finishing semiconductor devices.

However, recently minimum finishing dimensions (minimum finishing conditions of gates) have become equal to or less than wavelength levels of light used in lithography, and further

miniaturization of dimensions finishing is becoming more difficult.

Using the fact that the electron mobility (effective mass) changes when silicon crystals are strained, a method has been proposed in which silicon germanium, which has a larger lattice constant than silicon, is used for a substrate film for forming field-effect transistors, and a silicon layer is epitaxially grown thereon, whereby strain is imparted to the silicon serving as a channel portion, the mobility is raised, and the speed of the transistors is increased, as disclosed in JP-A-11-340337.

Also, a method in which the start-up delay of drain currents is controlled by stress control of the gate electrodes of field-effect transistors is disclosed in JP-A-6-232170.

In semiconductor devices in recent years, increases in the working speed of field-effect transistors have been achieved. As one means therefor, a method is being considered in which a silicon germanium material, which has a larger lattice constant that silicon, is used for a silicon substrate of channel portions, to thereby impart strain to the silicon and raise the mobility. This is being considered.

However, when materials having different crystal lattice constants are epitaxially grown so that the lattices are aligned, as disclosed in JP-A-11-340337, the energy of the strain generated in the crystal is large. With respect to a film thickness that is equal to or greater than a critical film thickness, there is the problem that rearrangement is generated in the crystal, and in processes

for manufacturing semiconductor devices such as LSI, there is an increase in the cost accompanying the introduction of new semiconductor devices, resulting from the introduction of uncommon materials, such as silicon germanium, so that practical utilization of this technique is not easy.

Also, complementary field-effect transistors are configured by formed of n-channel field-effect transistors using electrons as a carrier, and p-channel field-effect transistors using positive holes as a carriers, and so it is preferable to increase the speeds of both the n-channel field-effect transistors and the p-channel field-effect transistors in order to increase the speed of the semiconductor device as a whole.

In JP-A-6-232170, the target transistor is disclosed as a transistor created by a chemical semiconductor. Currently, consideration is not being given to transistors created on a silicon substrate as mainly used in LSI and a DRAM. The field-effect transistors therein are only n-channel field-effect transistors, and so consideration is only given to one axis with respect to the control direction of the stress, and the transistors have been insufficient.

The direction (direction in which the drain currents mainly flow) of the channels of field-effect transistors formed on the a silicon substrate is commonly disposed in aligned with a direction parallel to a <110> crystal axis. However, the development of complementary field-effect transistors, in which the channel

direction is used as the <100> crystal axis direction, is advancing from the standpoint of increasing the speed of a p-channel field-effect transistor (Hirokazu Sayama and Yasuaki Inoue, *Oyo Butsuri* ("Applied Physics"), Vol. 69, No. 9, p. 1099 (2000)). The mechanism by which the speed of the p-channel field-effect transistors is increased is thought to result from the hole mobility of positive hole of the <100> crystal axis being greater in comparison to that of the <110> axis, and short channel characteristics being improved.

However, the difference in the crystal axes is not only that ideal mobility (no strain) of the silicon crystal changes, but there is the potential for sensitivity with respect to stress (strain) to also change. In other words, there is the potential for the drain current (mobility), which is increased by tensile strain in <110> axis transistors, to be lowered in <100> axis transistors.

Therefore, in means for increasing speed by straining the crystal, the transistors whose channel direction is the <100> axis direction may be different from field-effect transistors whose channel direction is the <110> axis direction that are commonly considered.

SUMMARY OF THE INVENTION

It is an object of the invention to effectively realize, in a semiconductor device including n-channel field-effect

transistors and p-channel field-effect transistors, whose channel direction is a <100> axis direction, a semiconductor device in which drain current characteristics of the n-channel field-effect transistors and the p-channel field-effect transistors are excellent.

The present inventors measured stress dependency of drain currents of field-effect transistors whose channel direction is the <100> axis direction, and demonstrated that the stress dependency thereof is different that of transistors of the common <110> axis direction.

Fig. 2 is a graph showing experimental results of stress dependency of drain currents of n-channel field-effect transistors and p-channel field-effect transistors formed on an Si (001) surface so that the drain currents flow parallel to the <100> axis. The gate length of the evaluated field-effect transistors was 0.2 μm. The directions of the stress were uniaxial stress (stress parallel to the channels) within the channel surface in a direction parallel to the drain currents flowing through the channels of the field-effect transistors and uniaxial stress (stress orthogonal to the channels) within the channel surface in a direction orthogonal to the drain currents. With respect to the reference numerals of the stress, plus represents tensile stress and minus represents compression stress.

In Fig. 2, in the case of the n-channel field-effect

transistors, the drain currents increased with respect to tensile stress (stress parallel to the channels was about 4.3%/100 MPa, and stress orthogonal to the channels was about 0.85%/100 MPa).

In the case of the p-channel field-effect transistors, the drain currents increased with respect to compression stress (stress parallel to the channels was about 0.41%/100 MPa, and stress orthogonal to the channels was about 2.2%/100 MPa).

Fig. 3 illustrates results when an experiment that was the same as the above-described experiment was conducted in regard to transistors whose channel direction was the <110> direction.

In Fig. 3, in the case of the n-channel field-effect transistors, the drain currents increased with respect to tensile stress (stress parallel to the channels was about 4.3%/100 MPa, and stress orthogonal to the channels was about 1.7%/100 MPa).

In the case of the p-channel field-effect transistors, the drain currents increased with respect to the direction orthogonal to the channels (about 3.6%/100 MPa), but the drain currents decreased with respect to the direction parallel to the channels (about 6.3%/100 MPa).

As is clear from Figs. 2 and 3, it will be understood that stress dependency of the drain currents differs greatly depending on the channel direction. In particular, the

difference in dependency in p-channel field-effect transistors is great, and when transistors that are parallel to the <100> axis are created with the same stress control as transistors parallel to the <110> axis, it is thought that there is the potential for the drain currents to be reduced.

In other words, it was demonstrated that, in order to increase the drain current of transistors whose channel direction is the <110> axis direction, tensile stress should be loaded to the n-channel field-effect transistors in directions parallel and orthogonal to the inside of the channel surface, and compression stress should be loaded to the p-channel field-effect transistors in directions parallel and orthogonal to the inside of the channel surface.

In the debate within elastic deformation, stress and strain are in a proportional relation. Therefore, in the aforementioned experimental results, the reason that the drain current increases when tensile stress is loaded to the n-channel field-effect transistors parallel to the channel is believed to be because the crystal lattice of the silicon configuring the channel is strained in a tensile direction parallel to the inside of the channel in comparison with prior to loading the stress, whereby electron mobility increases. It is possible to measure this strain generated in the silicon crystal by TEM, electron beam analysis, and Raman spectrometry.

In multilayer film laminate structures, such as

transistors, thermal stress resulting from differences in the coefficient of linear expansion between the materials and inherent stress resulting from differences in the lattice constant and film contraction at the time of crystallization are generated, and residual stress is generated in the structure interior. Generations of field-effect transistors whose miniaturization has advanced over the years are commonly expressed by their gate lengths.

The present inventors demonstrated that, when stress analysis of field-effect transistor structures is conducted and reduction of the manufacturing dimensions of the gates advances, stress generated in the interiors of the structures becomes large due to the miniaturization of the structures and the use of new materials. Particularly, in field-effect transistors which belong to the generation having a 0.1 μm gate length, stress stemming from oxidation due to STIs (Shallow Trench Isolations) becomes a source of stress.

Fig. 4 is a graph showing results in which the stress of channel portions of each generation of gate length is analyzed by the finite element method. In Fig. 4, stress generated in channel portions under the gate is low in a transistor belonging to the generation in which the gate length is a comparatively large 2 μm. However, stress becomes drastically higher in a transistor belonging to the generation in which the gate length is 0.25 μm or less, and reaches almost 3 times that of the 2 μm generation in the 0.1

μm generation. Research is being conducted in regard to the influence of stress generated in field-effect transistors on transistor characteristics. For example, research is being conducted in regard to stress dependency of mutual conductance, which is one characteristic of field-effect transistors (Akemi Hamada, et al., *IEEE Trans. Electron Devices*, Vol. 38, No. 4, pp. 895-900, 1991).

However, conventionally, there was not the problem of the characteristics of field-effect transistors fluctuating due to stress. This is thought to be because, as shown in Fig. 4, stress generated in transistor structures was small in pre-0.25 μm field-effect transistors, i.e., of 0.25 μm or greater.

Moreover, it is also conceivable that sensitivity of the transistors themselves with respect to stress was also low.

Thus, when the present invention is adapted to a semiconductor device whose gate length is 0.25 μm or lower, it proves effective and is preferable.

Fig. 5 is a graph in which experimental results (gate length: 2 μm) of stress dependency of mutual conductance Gm of the aforementioned reference (Akemi Hamada, et al., *IEEE Trans. Electron Devices*, Vol. 38, No. 4, pp. 895-900, 1991) are compared with experimental results (gate length: 0.2 μm) of stress dependency of Gm of the inventors.

The comparison in Fig. 5 was conducted by loading stress

in a direction parallel to the channel with respect to n-channel field-effect transistors in which the channel was parallel to the <110> crystal axis. The dependency of Gm with respect to stress was about four times larger in the transistors of the generation in which the gate length was 0.2 μm than the transistors of the generation in which the gate length was 2 μm. That is, the comparison illustrates that the sensitivity of transistor characteristics with respect to stress becomes higher due to the generations of the transistors advancing.

According to stress analysis, with respect to stress distribution in the substrate depth direction formed in the channel portion of an Si substrate of a field-effect transistor, a place at which stress concentrates is formed near the gate electrode. The diffusion zone formation region of a transistor of the generation in which the gate length is a small 0.1 μm is formed in a shallow region near the substrate surface in comparison to a conventional transistor of a large gate length. As a result, it is conceivable that, in transistors of the 0.1 μm generation, device movement regions are easily influenced by stress.

Thus, the present inventors conducted stress analysis with the finite element method in regard to field-effect transistor structures having a gate length of 0.08 μm, and conducted sensitivity analysis in regard to the influence that materials configuring field-effect transistors and peripheral